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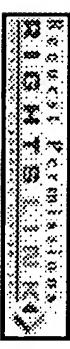
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# Flash memory BIOS for PC and notebook computers

Intel Corp., Folsom, CA, USA;

This paper appears in: Communications, Computers and Signal Processing, 1991., IEEE **Pacific Rim Conference on** 

Publication Date: 9-10 May 1991

On page(s): 692 - 695 vol.2

Meeting Date: 05/09/1991 - 05/10/1991

INSPEC Accession Number: 4208870 Location: Victoria, BC

Posted online: 2002-08-06 17:47:24.0 Digital Object Identifier: 10.1109/PACRIM.1991.160834

Abstract

increasing computer complexity requires rapid and convenient BIOS modifications. BIOS code can be stored in ROM, EPROM, EEPROM, controller is an ideal storage medium for PC and notebook computer BIOS code internal program and erase sequence controller. A 1-Mb block erasable flash memory with an providing boot and recovery code protected from inadvertent program or erasure. BIOS code is easily updated in flash memory containing an memory with update software provided on a desk or by modem. Block erasable flash memory provides the capability of BIOS updates while BIOS storage does not require EEPROM's feature of byte erasure. Rapid and inexpensive BIOS revisions can be accomplished in flash bulk erasable flash memory, or block erasable flash memory. Updating BIOS stored in ROM or EPROM requires much time and money. The author describes a flash memory device used to store the basic input/output system (BiOS) of a PC or notebook computer. Rapidly internal program and erase sequence

index ferms

Controlled Indexing

digital storage input-output programs microcomputers

Non-controlled Indexing

memory 1 MB BIOS code BIOS updates boot code builk erasable flash memory erase sequence controller flash memory device internal EEPROM EPROM PC ROM basic input/output system block erasable flash

mentoria natebook computers personal computers recovery code update software

**Author Keywords** 

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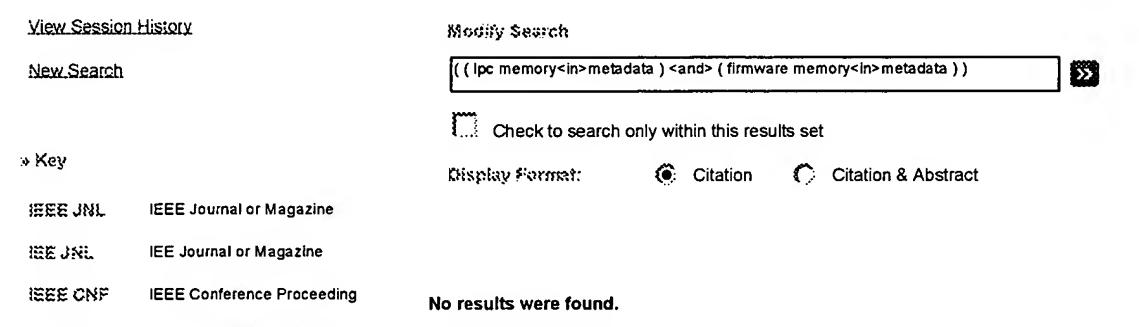
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<u>L5</u>	(firmware near5 memory) same (flag or pointer)	237	<u>L5</u>
<u>L4</u>	(LPC near5 memory) same (flag or pointer)	16	<u>L4</u>
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(LPC near5 memory) and (firmware near5 memory)	0

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<u>L10</u>	((LPC near5 memory) same (flag or pointer)) and (firmware near5 memory)	1	<u>L10</u>
<u>L9</u>	((LPC near5 memory) same (flag or pointer)) and((firmware near5 memory) same (flag or pointer))	. 1	<u>L9</u>
<u>L8</u>	17 and firmware	2	<u>L8</u>
<u>L7</u>	14 or L6	18	<u>L7</u>
<u>L6</u>	("low pin count" near5 memory) same (flag or pointer)	3	<u>L6</u>
<u>L5</u>	(firmware near5 memory) same (flag or pointer)	237	<u>L5</u>
<u>L4</u>	(LPC near5 memory) same (flag or pointer)	16	<u>L4</u>
<u>L3</u>	(LPC near5 memory) same (firmware near5 memory) same (flag or pointer)	1	<u>L3</u>
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DB=P	GPB, USPT, USOC; PLUR=YES; OP=OR		
<u>L1</u>	(LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer)	1	<u>L1</u>

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Terms	
(("low pin count" or LPC) near5 memory) same ((firmware or BIOS) near5 memory)	26

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L2 (("low pin count" or LPC) near5 memory) same ((firmware or BIOS) near5 memory) 26 L2

(("low pin count" or LPC) near5 memory) and ((firmware or BIOS) near5 memory)

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<u>L1</u>

44

<u>L1</u>

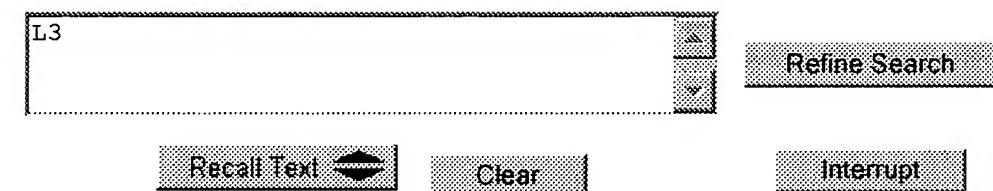
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<u>L3</u> L2	0	<u>L3</u>
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<u>L2</u> (("low pin count" or LPC) near5 memory) same ((firmware or BIOS) near5 memory)	) 26	<u>L2</u>
L1 (("low pin count" or LPC) near5 memory) and ((firmware or BIOS) near5 memory)	44	<u>L1</u>

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(LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer) <u>L1</u>

<u>L1</u>

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Terms		
(LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer)	0	

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L2 (LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer) 0 L2

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L1 (LPC adj1 memory) same (firmware adj1 memory) same (flag or pointer) 1 L1